Please cancel claims 1-3.

Please add claims 4-22 as follows:

--4. A method for self-routing a packet through a $b2^n \times b2^n$ switching network comprising

configuring the switching network with (a) 2^n output groups, each of the output groups having a distinct binary address in the form of $b_1 b_2 \ldots b_n$ with b indistinguishable output ports, and (b) k super-stages of concentrators wherein each of the concentrators is a $2b \times 2b$ partial sorting network of interconnected routing cells and b of its 2b output ports are grouped into a 0-output group while the remaining b output ports are grouped into a 1-output group, the network being characterized by the guide $\gamma(1), \gamma(2), \ldots, \gamma(k)$, where γ is a mapping from the set $\{1, 2, \ldots, k\}$ to the set $\{1, 2, \ldots, n\}$, and wherein the packet is either a real data packet destined for the output group at the binary destination address $d_1 d_2 \ldots d_n$, or an idle packet having no pre-determined destination,

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generating a routing tag $1d_{\gamma(1)}d_{\gamma(2)}\ldots d_{\gamma(k)}$ for the real data packet with reference to the guide of the network and the destination address of the packet, and

routing the real data packet through the network by using $1d_{\gamma(j)}$ in the routing tag in the j-th super-stage concentrator, $1 \leq j \leq k$, to select between the 0-output group or the 1-output group of the j-th super-stage concentrator to emit the real data packet.

5. A method for self-routing a packet through a $b2^n \times b2^n$ switching network, the network: including 2^n output groups, each of the output groups having a distinct binary

address in the form of $b_1b_2 \ldots b_n$ with b indistinguishable output ports, and k super-stages of concentrators wherein each of the concentrators is a 2b×2b partial sorting network of interconnected routing cells and b of its 2b output ports are grouped into a 0-output group while the remaining b output ports are grouped into a 1-output group; and being characterized by the guide $\gamma(1), \gamma(2), \ldots, \gamma(k)$, where γ is a mapping from the set $\{1, 2, \ldots, k\}$ to the set $\{1, 2, \ldots, n\}$, and wherein the packet is either a real data packet destined for the output group at the binary destination address $d_1d_2 \ldots d_n$, or an idle packet having no pre-determined destination, the method comprising

generating the routing tag $1d_{\gamma(1)}d_{\gamma(2)} \ldots d_{\gamma(k)}$ for the real data packet with reference to the guide of the network and the destination address of the packet, and

routing the real data packet through the network by using $1d_{\gamma(j)}$ in the routing tag in the j-th super-stage concentrator, $1 \leq j \leq k$, to select between the 0-output group or the 1-output group of the j-th super-stage concentrator to emit the real data packet.

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6. A method for self-routing a plurality of real data packets through a $b2^n \times b2^n$ switching network, the switching network being characterized by the guide $\gamma(1), \gamma(2), \ldots, \gamma(k)$ where γ is a mapping from the set $\{1, 2, \ldots, k\}$ to the set $\{1, 2, \ldots, n\}$, and having (a) $b2^n$ external input ports, (b) 2^n output groups, each of the output groups having a distinct binary address in the form of $b_1b_2 \ldots b_n$ with b indistinguishable output ports, and (c) k super-stages of 2b-to-b concentrators wherein each of the concentrators is a 2b×2b partial sorting network of interconnected routing cells where each of the routing cells is a sorting cell associated with the partial order "10 ('0-bound') $\prec$ 00 ('idle') $\prec$ 11 ('1-

bound')", b of the 2b output ports of each of the concentrators are grouped into a 0-output group while the remaining b output ports are grouped into a 1-output group, and extra circuitry arranged at the output end of each of the concentrators wherein the extra circuitry is composed of 2b parallel 1×1 switching elements, one at each of the output ports of the concentrator, and each of the real data packets arriving at a distinct external input port determining an active input port and destined for an output group at the binary destination address $d_1d_2 \ldots d_n$, the method comprising

generating an idle packet as a stream of '0' bits at each of the non-active external input ports,

generating a routing tag $1d_{\gamma(1)}d_{\gamma(2)} \ldots d_{\gamma(k)}$ for each of the real data packets with reference to the guide of the network and the destination address of the packet,

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generating a routing tag which is a string of k+1 '0' bits for each of the idle packets,

routing the real data packets and the idle packets through the network by sorting the packets by the 2b-to-b concentrators of the network, wherein the sorting at each of the concentrators includes the sorting at each of the sorting cells of the concentrator such that the sorting is with respect to the associated partial order and is based upon the leading two bits, which are either '10' or '11' for a real data packet, or '00' for an idle packet, of the routing tag of each of the two packets arrived at each of the sorting cells, and

processing the routing tag of each of the packets by the extra circuitry at the output end of the concentrator before the said each of the packets exits from the j-th super-stage concentrator by removing the second leading bit from the routing tag or

rotating the second leading bit to the end of the routing tag such that the leading two bits of the routing tag of each of the packets at each of the j-th super-stage concentrators, $1 \leq j \leq k$, are always '$1d_{\gamma(j)}$' or '00'.

7. The method as recited in claim 6 wherein the real data packets are classified into 2^r priority classes, $r \geq 1$, wherein each of the priority classes is coded in an r-bit string $p_1 \ldots p_r$, and the generating of a routing tag for each of the real data packets includes generating $1d_{\gamma(1)}p_1 \ldots p_r d_{\gamma(2)} \ldots d_{\gamma(k)}$ as the routing tag.

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8. The method as recited in claim 6 wherein the generating of a routing tag for each of the idle packets includes generating a string of k+r+1 '0' bits as the routing tag.

9. The method as recited in claim 6 wherein each of the priority classes is coded in an r-bit string $p_1 \ldots p_r$, the generating of a routing tag for each of the real data packets includes generating $1d_{\gamma(1)}p_1 \ldots p_r d_{\gamma(2)} \ldots d_{\gamma(k)}$ as the routing tag, the sorting at each of the sorting cells of the concentrator based upon the two leading bits of the routing tag includes using the priority code $p_1 \ldots p_r$ as the tiebreaker, and processing the routing tag includes generating the routing tag such that the leading r+2 bits of the routing tag of each of the real data packets at each of the j-th super-stage concentrators, $1 \leq j \leq k$, is '$1d_{\gamma(j)}p_1 \ldots p_r$'.

10. The method as recited in claim 6 wherein the real data packets are classified into 2^r priority classes, $r \geq 1$, wherein each of the priority classes is coded in an r-bit string

$p_1 \ldots p_r$, the generating of a routing tag for each of the real data packets includes generating $1d_{\gamma(1)}p_1 \ldots p_r d_{\gamma(2)} \ldots d_{\gamma(k)}$ as the routing tag, the generating of a routing tag for each of the idle packets includes generating a string of k+r+1 '0' bits as the routing tag, the sorting at each of the sorting cells of the concentrator based upon the two leading bits of the routing tag includes using the priority code $p_1 \ldots p_r$ as the tiebreaker, and processing the routing tag includes removing the second leading bit from the routing tag or rotating the second leading bit to the end of the routing tag, and rotating the r-bit priority code $p_1 \ldots p_r$ to the position behind the next bit originally following the priority code in the routing tag such that the leading r+2 bits of the routing tag of each of the packets at each of the j-th super-stage concentrators, $1 \leq j \leq k$, are always '$1d_{\gamma(j)}p_1 \ldots p_r$' or '00…0'.

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11. The method as recited in claim 6 wherein the routing of packets includes changing the leading two bits of the routing tag of a misrouted packet into the new value "01" at the output end of a 2b-to-b concentrator at a super-stage upon output contention, and using the new value throughout the remaining stages, and the sorting at each of the sorting cells of each of the concentrator is with respect to the partial order "10 ('0-bound') $\prec$ 0x ('idle' or 'misrouted') $\prec$ 11 ('1-bound')".

12. The method as recited in claim 6 wherein the routing of the real data packets includes blocking misrouted packets at the output end of each of the 2b-to-b concentrators upon output contention.

13. The method as recited in claim 12 wherein the blocking of the misrouted packets includes turning each of the misrouted packets into a string of '0' bits as an idle packet.

14. A system for self-routing a packet comprising

a $b2^n \times b2^n$ switching network, the switching network having (a) 2^n output groups, each of the output groups having a distinct binary address in the form of $b_1 b_2 \ldots b_n$ with b indistinguishable output ports, and (b) k super-stages of concentrators wherein each of the concentrators is a $2b \times 2b$ partial sorting network of interconnected routing cells and b of its 2b output ports are grouped into a 0-output group while the remaining b output ports are grouped into a 1-output group, the network being characterized by the guide $\gamma(1), \gamma(2), \ldots, \gamma(k)$, where γ is a mapping from the set $\{1, 2, \ldots, k\}$ to the set $\{1, 2, \ldots, n\}$, and wherein the packet is either a real data packet destined for the output group at the binary destination address $d_1 d_2 \ldots d_n$, or an idle packet having no pre-determined destination,

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routing tag circuitry for generating a routing tag $1d_{\gamma(1)}d_{\gamma(2)}\ldots d_{\gamma(k)}$ for the real data packet with reference to the guide of the network and the destination address of the packet, and

routing control circuitry for routing the real data packet through the network by using $1d_{\gamma(j)}$ in the routing tag in the j-th super-stage concentrator, $1 \leq j \leq k$, to select between the 0-output group or the 1-output group of the j-th super-stage concentrator to emit the real data packet.

1~~5~~. A system for self-routing a plurality of real data packets comprising

a $b2^n \times b2^n$ switching network having a plurality of 2b-to-b concentrators interconnected into a k-stage bit-permuting network characterized by guide $\gamma(1), \gamma(2), \ldots, \gamma(k)$ where γ is a mapping from the set $\{1, 2, \ldots, k\}$ to the set $\{1, 2, \ldots, n\}$, and having (a) $b2^n$ external input ports, (b) 2^n output groups, each of the output groups having a distinct binary address in the form of $b_1b_2\ldots b_n$ with b indistinguishable output ports, and (c) k super-stages of 2b-to-b concentrators wherein each of the concentrators is a $2b\times 2b$ partial sorting network of interconnected routing cells where each of the routing cells is a sorting cell associated with the partial order "10 ('0-bound') $\prec$ 00 ('idle') $\prec$ 11 ('1-bound')", b of the 2b output ports of each of the concentrators are grouped into a 0-output group while the remaining b output ports are grouped into a 1-output group, and extra circuitry arranged at the output end of each of the concentrators wherein the extra circuitry is composed of 2b parallel 1×1 switching elements, one at each of the output ports of the concentrator, and wherein each of the real data packets arrives at a distinct external input port and is destined for an output group at the binary destination address $d_1d_2\ldots d_n$,

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idle-packet-generating circuitry, coupled to the external input ports, for generating an idle packet as a stream of '0' bits at each of the external input ports of the switching network if no real data packet arrived at that external input port,

routing tag circuitry, coupled to the external input ports, for generating a routing tag $1d_{\gamma(1)}d_{\gamma(2)}\ldots d_{\gamma(k)}$ for each of the real data packets with reference to the guide of the network and the destination address of the packet, or generating a routing tag which is a string of k+1 '0' bits for each of the idle packets,

routing control circuitry, coupled to the concentrators, for routing the real data packets and the idle packets through the network by sorting the packets by the 2b-to-b concentrators of the network, wherein the sorting at each of the concentrators includes the sorting at each of the sorting cells of the concentrator where the sorting is with respect to the associated partial order and is based upon the leading two bits, which are either '10' or '11' for a real data packet, or '00' for an idle packet, of the routing tag of each of the two packets arrived at the cell, and

extra circuitry at the output end of the j-th super-stage concentrator, $1 \leq j \leq k$, for processing the routing tag of each of the packets before the said each of the packets exits from the j-th super-stage concentrator by removing the second leading bit from the routing tag or rotating the second leading bit to the end of the routing tag such that the leading two bits of the routing tag of each of the packets at each of the j-th super-stage concentrators, $1 \leq j \leq k$, are always '$1d_{\gamma(j)}$' or '00'.

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16. The system as recited in claim 15 wherein the real data packets are classified into 2^r priority classes, $r \geq 1$, wherein each of the priority classes is coded in an r-bit string $p_1 \ldots p_r$, and the routing tag circuitry for each of the real data packets includes means for generating $1d_{\gamma(1)}p_1 \ldots p_r d_{\gamma(2)} \ldots d_{\gamma(k)}$ as the routing tag.

17. The system as recited in claim 15 wherein the idle-packet-generating circuitry includes means for generating a string of k+r+1 '0' bits as the routing tag.

18. The system as recited in claim 15 wherein each of the priority classes is coded in an r-bit string $p_1 \ldots p_r$, the routing tag circuitry for each of the real data packets includes means for generating $1d_{\gamma(1)}p_1 \ldots p_r d_{\gamma(2)} \ldots d_{\gamma(k)}$ as the routing tag, the routing control circuitry includes means using the priority code $p_1 \ldots p_r$ as the tiebreaker, and the extra circuitry includes means for generating the routing tag such that the leading r+2 bits of the routing tag of each of the real data packets at each of the j-th super-stage concentrators, $1 \le j \le k$, is '$1d_{\gamma(j)}p_1 \ldots p_r$'.

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19. The system as recited in claim 15 wherein the real data packets are classified into 2^r priority classes, $r \ge 1$, wherein each of the priority classes is coded in an r-bit string $p_1 \ldots p_r$, the routing tag circuitry generates $1d_{\gamma(1)}p_1 \ldots p_r d_{\gamma(2)} \ldots d_{\gamma(k)}$ as the routing tag for each of the real data packets, and a string of k+r+1 '0' bits as the routing tag for each of the idle packets, the routing control circuitry includes means for sorting the two arriving packets based upon the two leading bits of the routing tags of the two packets using the ensuing priority code $p_1 \ldots p_r$ as the tiebreaker, and the extra circuitry at the output end of the concentrator processes the routing tag of each of the packets before the said each of the packets exits from the j-th super-stage concentrator by removing the second leading bit from the routing tag or rotating the second leading bit to the end of the routing tag, and rotating the r-bit priority code $p_1 \ldots p_r$ to the position behind the next bit originally following the priority code in the routing tag such that the leading r+2 bits of the routing tag of each of the packets at each of the j-th super-stage concentrators, $1 \le j \le k$, are always '$1d_{\gamma(j)}p_1 \ldots p_r$' or '00…0'.

20. The system as recited in claim 15 wherein the switch includes delay elements in the 2b-to-b concentrator for maintaining the synchronization of the packets across the stage.

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21. The system as recited in claim 15 wherein the extra circuitry at the output end of each of the 2b-to-b concentrators changes the leading two bits of the routing tag of a misrouted packet into the new value "01" at a super-stage upon output contention, and the new value is used throughout the remaining stages, and each of the sorting cells of each of the concentrators is associated with the partial order "10 ('0-bound') $\prec$ 0x ('idle' or 'misrouted') $\prec$ 11 ('1-bound')".

22. The system as recited in claim 21 wherein the switch includes annihilators of misrouted packets at the output end of each of the 2b-to-b concentrators.--.